Further as shown in FIG. 27D, a groove is formed on the first temporary board 84A while the insulating layer 85 serves as a mask. Thereafter as shown in FIG. 27E, a conductive material layer 88 is deposited on the first temporary board 84A by a sputtering technique and the like, then as shown in FIG. 27F, the surface of the first temporary board 84A is polished by a CMP technique and the like. In such a manner, the conductive material layer 88 is embedded in the opening 87.

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In the Claims:

Please cancel claims 1-16, 20 and 22-24 without prejudice or disclaimer of the subject matter contained therein.

The following replacement claims are respectfully submitted:

17. (Amended) A method of fabricating an IC chip comprising:

laminating a first insulating layer on a board;

forming an electrode pad on the board, the electrode pad serving as an input/output terminal;

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laminating a second insulating layer over the board and the electrode pad;

forming a first resist pattern on the second insulating layer at a region other than a part of the electrode pad;

etching and removing the second insulating layer using the first resist pattern as a mask, thereby defining a first opening in the second insulating layer on the electrode

pad;

filling the first opening with a conductive material layer made of a conductive material;

laminating a third insulating layer over the second insulating layer and the conductive material layer;

forming a second resist pattern on the third insulating layer at a region other than a region of the conductive material layer;

B5 cont.

etching and removing the third insulating layer using the second resist pattern as a mask, thereby defining a second opening in the third insulating layer at the region of the conductive material layer;

filling the second opening with a metal layer made of an electric connection material; and

etching and removing the third insulating layer and the second insulating layer after said filling the second opening.

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19. (Amended) A method of fabricating an IC chip comprising:

laminating a first insulating layer on a board;

forming an electrode pad on the board, the electrode pad serving as an

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input/output terminal;

laminating a second insulating layer over the board and the electrode pad;

forming a resist pattern on the second insulating layer at a region other than a

part of the electrode pad;

first etching and removing of the second insulating layer using the resist pattern as a mask, thereby defining an opening in the second insulating layer on the electrode pad;

B6 cont. filling the opening with a conductive material layer made of a conductive material;

second etching and removing of the second insulating layer, thereby exposing a top and sidewalls of the conductive material layer; and

dipping a tip end of the exposed conductive material layer including the top and sidewalls thereof into a liquid bath filled with a molten electric connection material.

Please add claims as follows:

--25. The method of fabricating an IC chip according to claim 17, wherein the second resist pattern is formed so that the metal layer filled in the second opening is wider than the conductive material layer filled in the first opening.

B7 26. The method of fabricating an IC chip according to claim 17, wherein the second resist pattern is formed so that the metal layer filled in the second opening is narrower than the conductive material filled in the first opening.

27. The method of fabricating an IC chip according to claim 17, wherein the

second resist pattern is formed so that a width of the metal layer filled in the second opening is substantially the same as a width of the conductive material layer in the second opening.

28. The method of fabricating an IC chip according to claim 17, further comprising:

placing the board over a printed board after said etching and removing the third insulating layer and the second insulating layer, the electrode pad being aligned with a pad formed on the printed board; and

B7 cont.

heating the electric connection material to electrically connect the electrode pad with the pad formed on the printed board.

29. The method of fabricating an IC chip according to claim 28, wherein the electric connection material is solder.

30. The method of fabricating an IC chip according to claim 17, further comprising forming a filling insulating material on the first insulating layer and the electrode pad after said etching and removing the third insulating layer and the second insulating layer, to surround sidewalls of the conductive material layer and the metal layer.

31. The method of fabricating an IC chip according to claim 19, wherein said dipping comprises dipping the tip end into a plating bath filled with plating liquid.

32. The method of fabricating an IC chip according to claim 19, wherein said second etching and removing of the second insulating layer exposes all of the sidewalls of the conductive layer.

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33. The method of fabricating an IC chip according to claim 19, wherein portions of the sidewalls of the conductive material layer remain covered by the second insulating layer after said etching and removing of the second insulating layer.--